**Lab 6 – Arithmetic Unit**

CS1050 Computer Organization and Digital Design

Name : **Dissanayake D.M.A.K.**

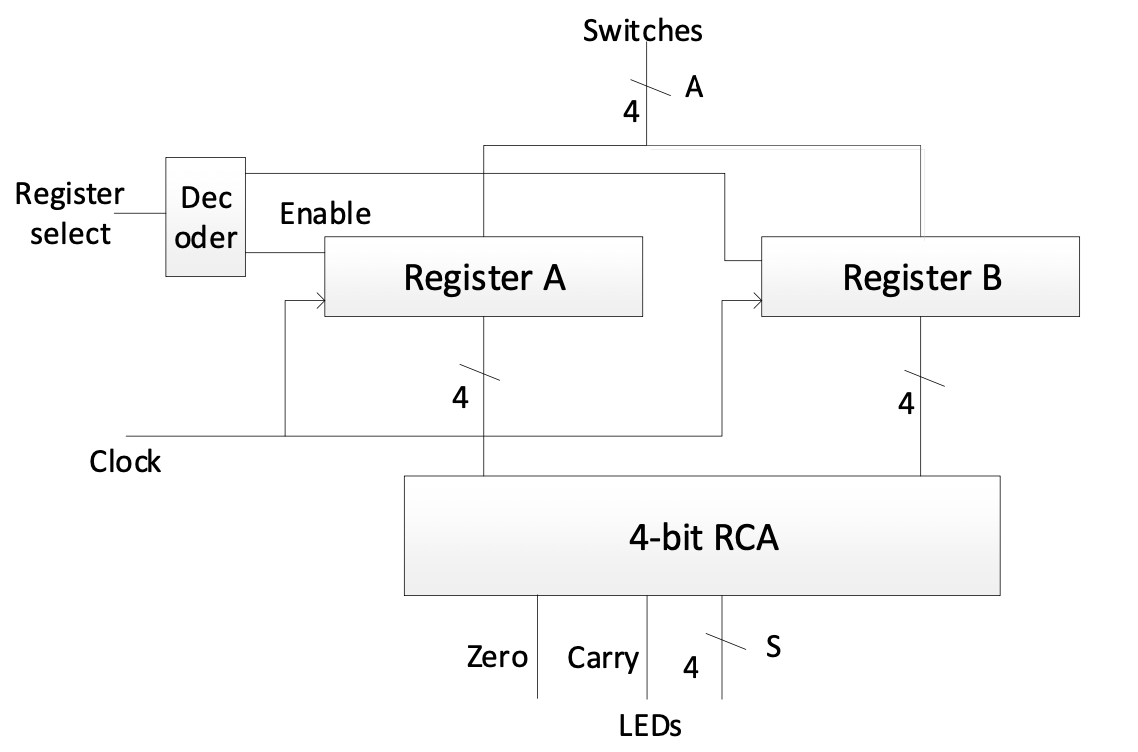
Index No. : **220135N**

Group : **44**

# Lab Task:

***Designing and Development of 4-bit register and 4-bit Arithmetic Unit run on Basys3 board.***

**Introduction**

**** In the realm of microprocessors, registers play a pivotal role as repositories for sets of bits. Our mission in this lab is to engineer a 4-bit Arithmetic Unit capable of performing additions on numbers housed in two separate registers. To grasp the intricacies of this task, we'll begin with the creation of a 4-bit register utilizing D Flip Flops. This register, featuring an Enable input and a Clock input, will set the stage for the subsequent integration with our 4-bit RCA.

**1)4-bit Register**

**Design Source File**

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-- Company:

-- Engineer:

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-- Create Date: 03/12/2024 02:07:04 PM

-- Design Name:

-- Module Name: Reg - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**entity** Reg **is**

**Port** **(** D **:** **in** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

En **:** **in** STD\_LOGIC**;**

Clk **:** **in** STD\_LOGIC**;**

Q **:** **out** STD\_LOGIC\_VECTOR **(**3 **downto** 0**));**

**end** Reg**;**

**architecture** Behavioral **of** Reg **is**

**begin**

**process** **(**Clk**)** **begin**

**if** **(rising\_edge(**Clk**))** **then**

**if** En **=** '1' **then**

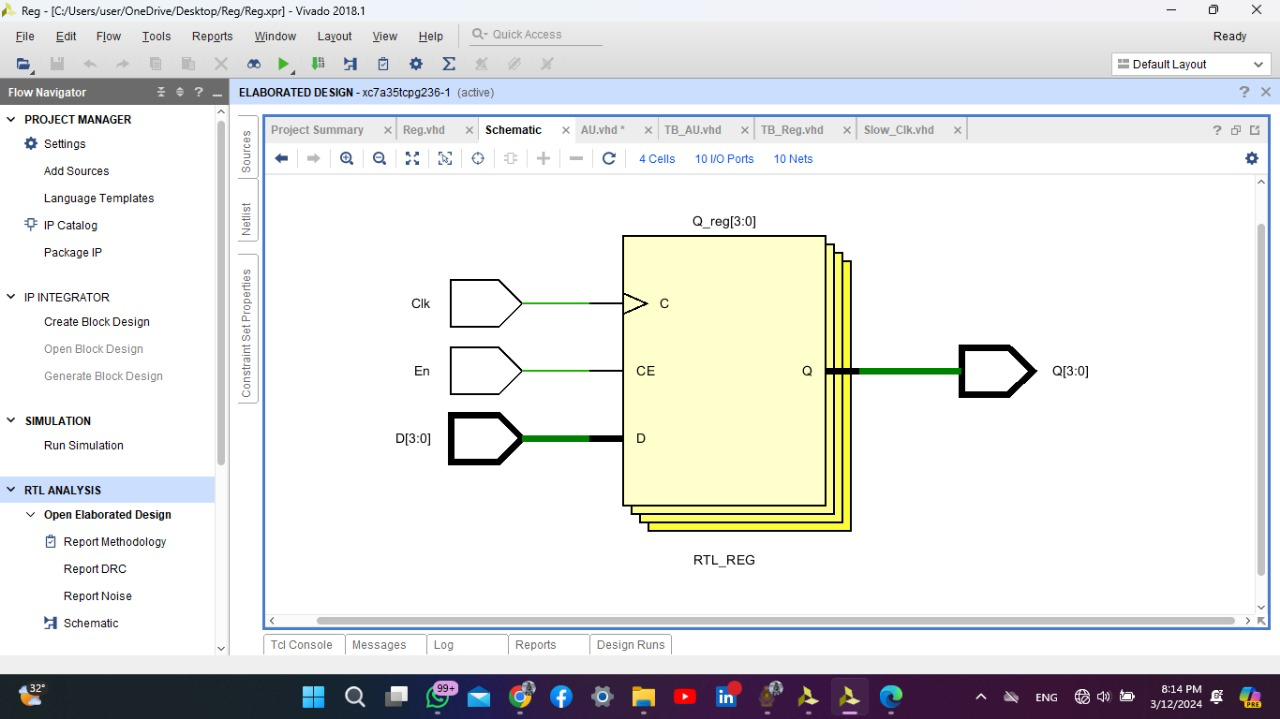
Q **<=** D**;**

**end** **if;**

**end** **if;**

**end** **process;**

**end** Behavioral**;**

**Elaborated design schematic**

**2)4-bit Arithmetic Unit**

**Design Source File**

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-- Company:

-- Engineer:

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-- Create Date: 03/12/2024 02:11:40 PM

-- Design Name:

-- Module Name: AU - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**entity** AU **is**

**Port** **(** A **:** **in** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

RegSel **:** **in** STD\_LOGIC**;**

Clk **:** **in** STD\_LOGIC**;**

S **:** **out** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

Zero **:** **out** STD\_LOGIC**;**

Carry **:** **out** STD\_LOGIC**);**

**end** AU**;**

**architecture** Behavioral **of** AU **is**

**component** Reg

**Port** **(** D **:** **in** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

En **:** **in** STD\_LOGIC**;**

Clk **:** **in** STD\_LOGIC**;**

Q **:** **out** STD\_LOGIC\_VECTOR **(**3 **downto** 0**));**

**end** **component;**

**component** RCA\_4

**Port** **(** A0 **:** **in** STD\_LOGIC**;**

A1 **:** **in** STD\_LOGIC**;**

A2 **:** **in** STD\_LOGIC**;**

A3 **:** **in** STD\_LOGIC**;**

B0 **:** **in** STD\_LOGIC**;**

B1 **:** **in** STD\_LOGIC**;**

B2 **:** **in** STD\_LOGIC**;**

B3 **:** **in** STD\_LOGIC**;**

C\_in **:** **in** STD\_LOGIC**;**

S0 **:** **out** STD\_LOGIC**;**

S1 **:** **out** STD\_LOGIC**;**

S2 **:** **out** STD\_LOGIC**;**

S3 **:** **out** STD\_LOGIC**;**

C\_out **:** **out** STD\_LOGIC**);**

**end** **component;**

**component** Slow\_Clk

**Port** **(** Clk\_in **:** **in** STD\_LOGIC**;**

Clk\_out **:** **out** STD\_LOGIC**);**

**end** **component;**

**signal** Enable\_A **:** STD\_LOGIC**;**

**signal** Enable\_B **:** STD\_LOGIC**;**

**signal** A\_out **:** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

**signal** B\_out **:** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

**signal** Clk\_Slow **:** STD\_LOGIC**;**

**begin**

--Logic of 1 to 2 decoder

Enable\_A **<=** **not** RegSel**;**

Enable\_B **<=** RegSel**;**

SLow\_Clk\_0 **:** Slow\_Clk

**port** **MAP** **(**Clk**,** Clk\_Slow**);**

Reg\_A **:** Reg

**port** **MAP** **(**

A**,**Enable\_A**,**Clk\_Slow**,**A\_out

**);**

Reg\_B **:** Reg

**port** **MAP** **(**

A**,**Enable\_B**,**Clk\_SLow**,**B\_out

**);**

RCA\_4\_0 **:** RCA\_4

**port** **MAP** **(**

A0 **=>** A\_out**(**0**),**

A1 **=>** A\_out**(**1**),**

A2 **=>** A\_out**(**2**),**

A3 **=>** A\_out**(**3**),**

B0 **=>** B\_out**(**0**),**

B1 **=>** B\_out**(**1**),**

B2 **=>** B\_out**(**2**),**

B3 **=>** B\_out**(**3**),**

C\_in **=>** '0'**,**

s0 **=>** S**(**0**),**

s1 **=>** S**(**1**),**

s2 **=>** S**(**2**),**

s3 **=>** S**(**3**),**

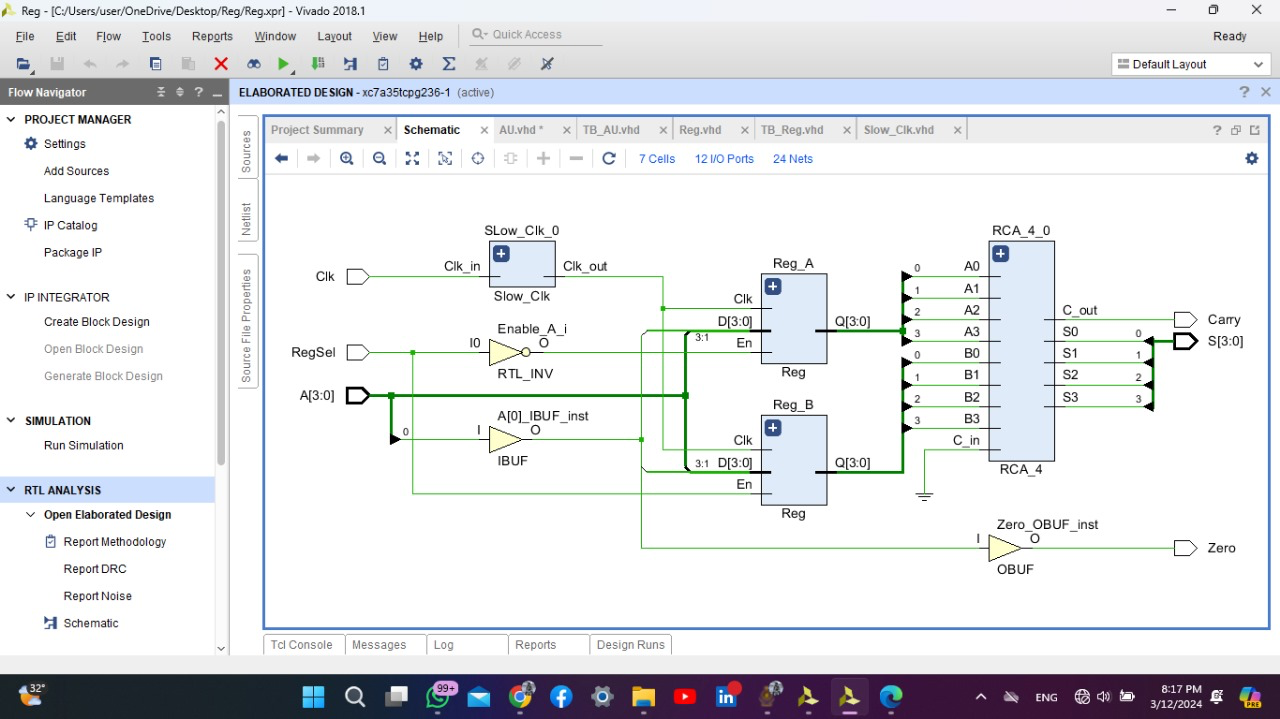
C\_out **=>** Carry

**);**

--logic for zero

Zero **<=** **(**A\_out**(**3**)** **xnor** B\_out**(**3**))** **and** **(**A\_out**(**2**)** **xnor** B\_out**(**2**))** **and** **(**A\_out**(**1**)** **xnor** B\_out**(**1**))** **and** **(**A\_out**(**0**)** **xnor** B\_out**(**0**));**

**end** Behavioral**;**

**Elaborated design schematic**

**Simulation source file**

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-- Company:

-- Engineer:

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-- Create Date: 03/12/2024 03:47:22 PM

-- Design Name:

-- Module Name: TB\_AU - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

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-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**entity** TB\_AU **is**

-- Port ( );

**end** TB\_AU**;**

**architecture** Behavioral **of** TB\_AU **is**

**component** AU

**Port** **(** A **:** **in** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

RegSel **:** **in** STD\_LOGIC**;**

Clk **:** **in** STD\_LOGIC**;**

S **:** **out** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

Zero **:** **out** STD\_LOGIC**;**

Carry **:** **out** STD\_LOGIC**);**

**end** **component;**

**signal** A **:** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

**signal** RegSel **:** STD\_LOGIC**;**

**signal** Clk **:** STD\_LOGIC**;**

**signal** S **:** STD\_LOGIC\_VECTOR **(**3 **downto** 0**);**

**signal** Zero **:** STD\_LOGIC**;**

**signal** Carry **:** STD\_LOGIC**;**

**begin**

UUT **:** AU

**PORT** **MAP** **(**A**,** RegSel**,** Clk**,** S**,** Zero**,** Carry**);**

Clk\_process**:** **process**

**begin**

Clk **<=** '0'**;** **wait** **for** 5ns**;**

Clk **<=** '1'**;** **wait** **for** 5ns**;**

**end** **process;**

**process**

**begin**

RegSel **<=** '0'**;**

A **<=** "0011"**;**

**wait** **for** 100ns**;**

RegSel **<=** '1'**;**

A **<=** "0001"**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

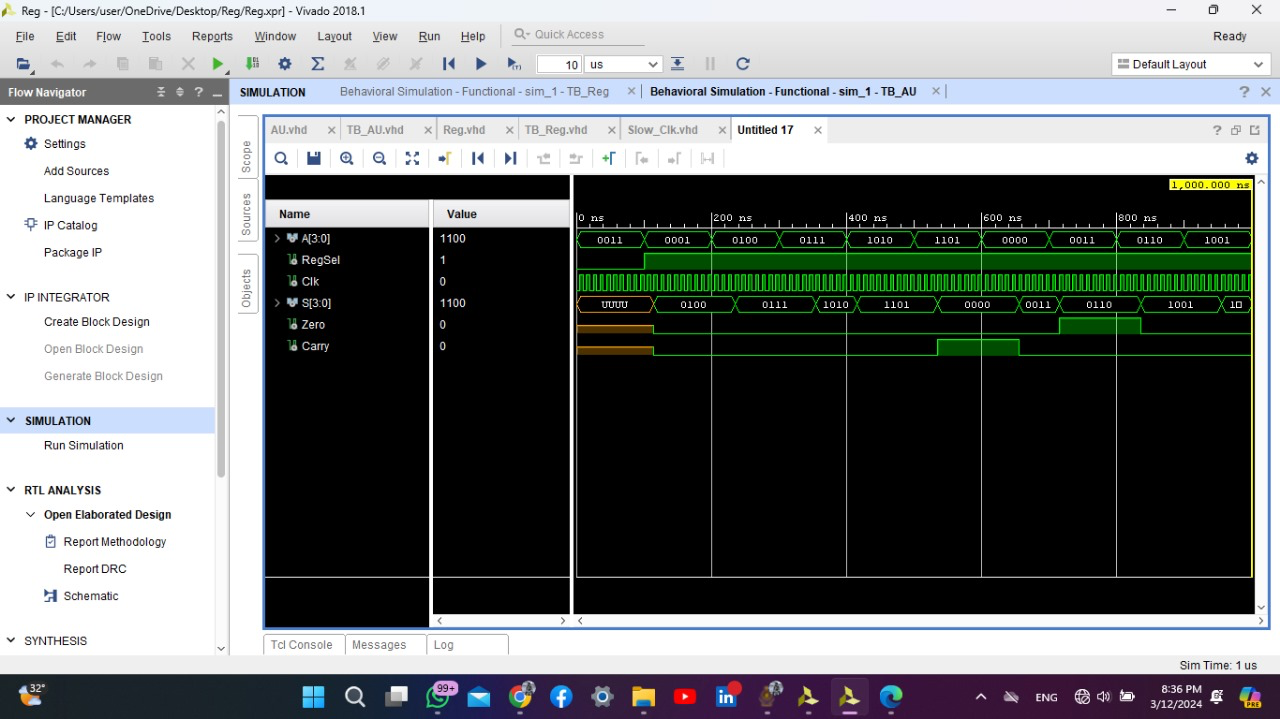
RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

RegSel **<=** '1'**;** A **<=** S**;** **wait** **for** 100ns**;**

**wait** **;**

**end** **process;**

**end** Behavioral**;**

**Timing Diagram**

A computer screen shot of a computer

Description automatically generated**Implemented design schematic**

**Constraints File**

## Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports Clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports Clk]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports Clk]

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {A[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {A[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[3]}]

set\_property PACKAGE\_PIN R2 [get\_ports {RegSel}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {RegSel}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {S[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[0]}]

set\_property PACKAGE\_PIN E19 [get\_ports {S[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[1]}]

set\_property PACKAGE\_PIN U19 [get\_ports {S[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[2]}]

set\_property PACKAGE\_PIN V19 [get\_ports {S[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[3]}]

set\_property PACKAGE\_PIN P1 [get\_ports {Carry}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Carry}]

set\_property PACKAGE\_PIN L1 [get\_ports {Zero}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {Zero}]

**Conclusion**

In conclusion, the 4-bit Arithmetic Unit (AU) crafted in this lab serves as a digital powerhouse capable of adding numbers stored in distinct registers. Similar to a counter's versatility, this AU exhibits flexibility by accommodating two registers, enabling users to input 4-bit binary values via switches. Functionality is orchestrated through clock synchronization, and the outcome of the addition process is vividly displayed on LEDs. Much like a counter measuring occurrences, this AU extends its utility to compute and showcase the sum of registered numbers, underscoring its significance in diverse electronic applications. The seamless integration of theoretical concepts with practical implementation in this lab not only enhances our understanding of digital design but also equips us with valuable skills for future endeavors in microprocessor architecture.

-End-